ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

ADF4356 Datasheet Update

Background

- Following a review of datasheet parameters, and to bring enhanced clarity to the operational performance of the part, some specifications have be updated and the production test accordingly enhanced.
- The max input frequency for 4/5 prescaler is reduced to 5.7GHz and 6GHz (see next slide for details).
- **NB➔ ADF4356 has not been altered (no changes to part fabrication, assembly). In most cases, customers can continue to use the part with same performance.**

Specification Change: RF Output Frequency

- New RF Output Characteristics are based on updated characterization and yield results
- Specifications have been clarified compared to previous datasheet revision

Updated

RF OUTPUT CHARACTERISTICS					
VCO Frequency Range		3400	6800	MHz	Fundamental VCO range
$RF_{OUT}A+/RF_{OUT}A-$ and $RF_{OUT}B+/RF_{OUT}B-$ Frequency		53.125	6800	MHz	Prescaler = 8/9
$RF_{OUT}A+/RF_{OUT}A-$ Frequency		53.125	6000	MHz	Prescaler = 4/5, $T_A \geq 25°C$
$RF_{OUT}A+/RF_{OUT}A-$ Frequency		53.125	5700	MHz	Prescaler = 4/5
$RF_{OUT}B+/RF_{OUT}B-$ Frequency		53.125	6800	MHz	Prescaler = 4/5, Divided Feedback to N counter with Output Divider ≥ 2
$RF_{OUT}B+/RF_{OUT}B-$ Frequency		53.125	6000	MHz	Prescaler = 4/5, Fundamental Feedback to N counter, $T_A \geq 25°C$
$RF_{OUT}B+/RF_{OUT}B-$ Frequency		53.125	5700	MHz	Prescaler = 4/5, Fundamental Feedback to N counter

Previously

RF OUTPUT CHARACTERISTICS					
VCO Frequency Range		3400	6800	MHz	Fundamental VCO range
RF Output Frequency		53.125	6800	MHz	

Prescaler Setting Explained

- A note has been added to explain how to set Prescaler Value

Updated:

Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRACx, and MODx counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (Bit DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 6 GHz when $T_A \geq 25$ and 5.7 GHz for all temperature range. It is still possible to generate frequencies up to 6.8 GHz from RF output B with prescaler 4/5 by enabling RF Output B Select bit (Bit DB25) in Register 6. The Feedback Select bit (DB24) in Register 6 is set to Divided and output divider is set to greater than 2. The prescaler limits the INT value; therefore, if P is 4/5, N_{MIN} is 23, and if P is 8/9, N_{MIN} is 75.

Previously:

Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRACx, and MODx counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (Bit DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 7 GHz. The prescaler limits the INT value; therefore, if P is 4/5, N_{MIN} is 23, and if P is 8/9, N_{MIN} is 75.